Rec'd PCT/PTO 29 MAR 2005
PCT/EP2003/011087
10/529527

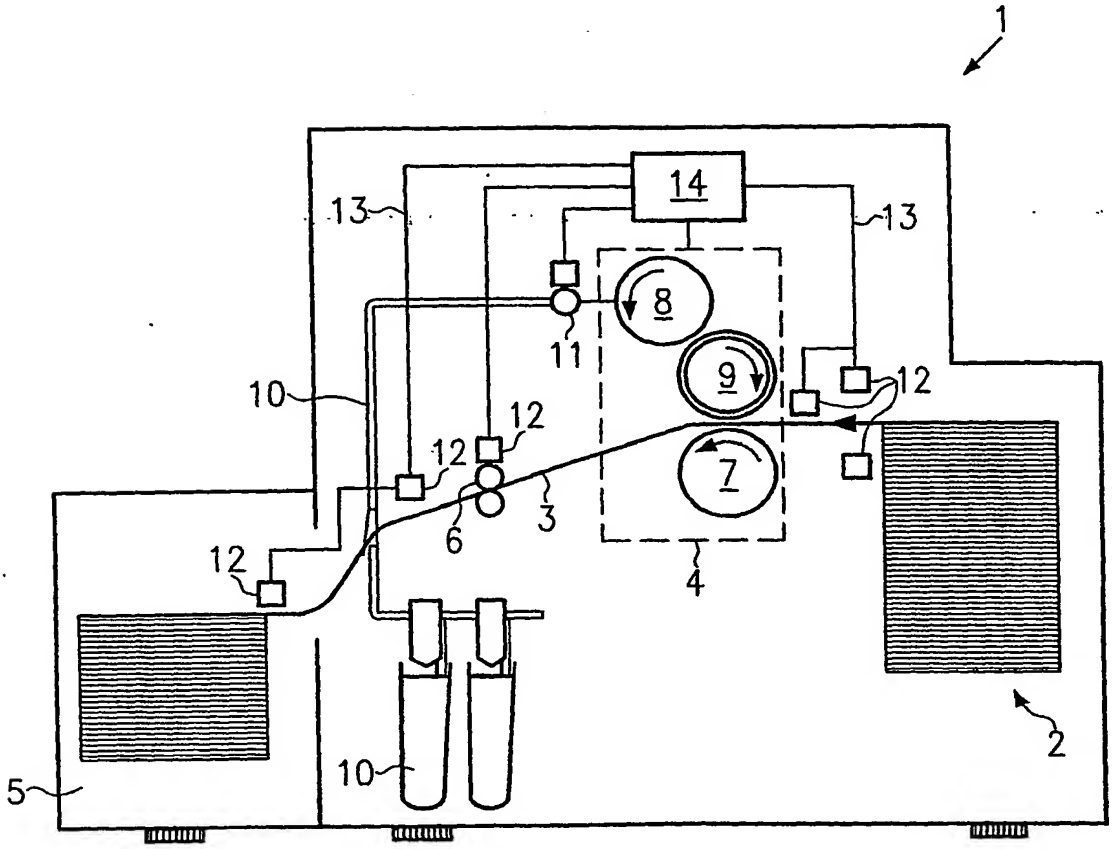


FIG. 1

Rec'd PCT/PTO 29 MAR 2005
PCT/EP2003/011087
10/529527

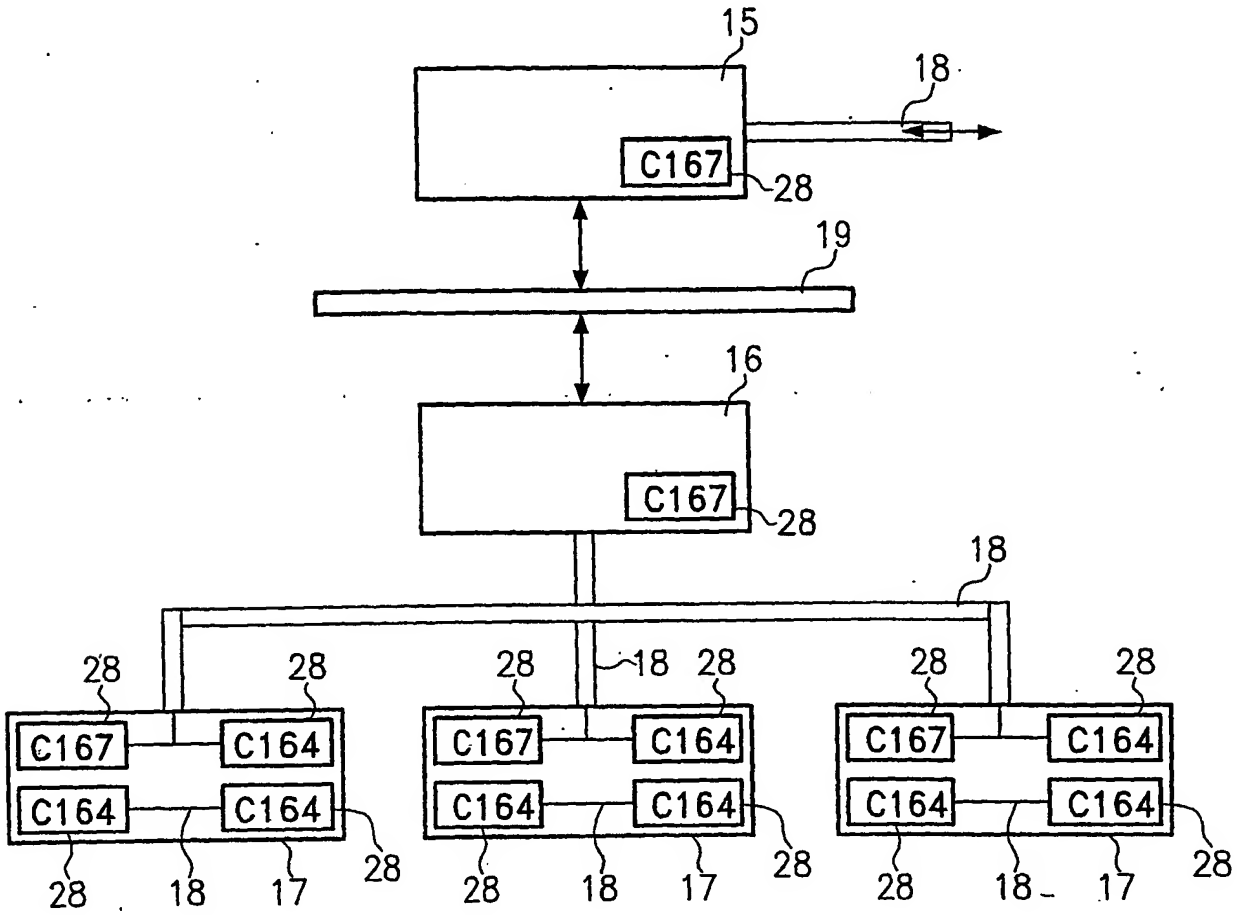


FIG.2

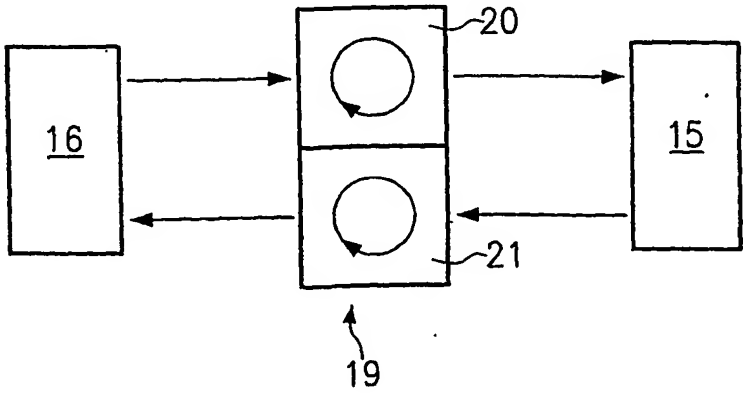
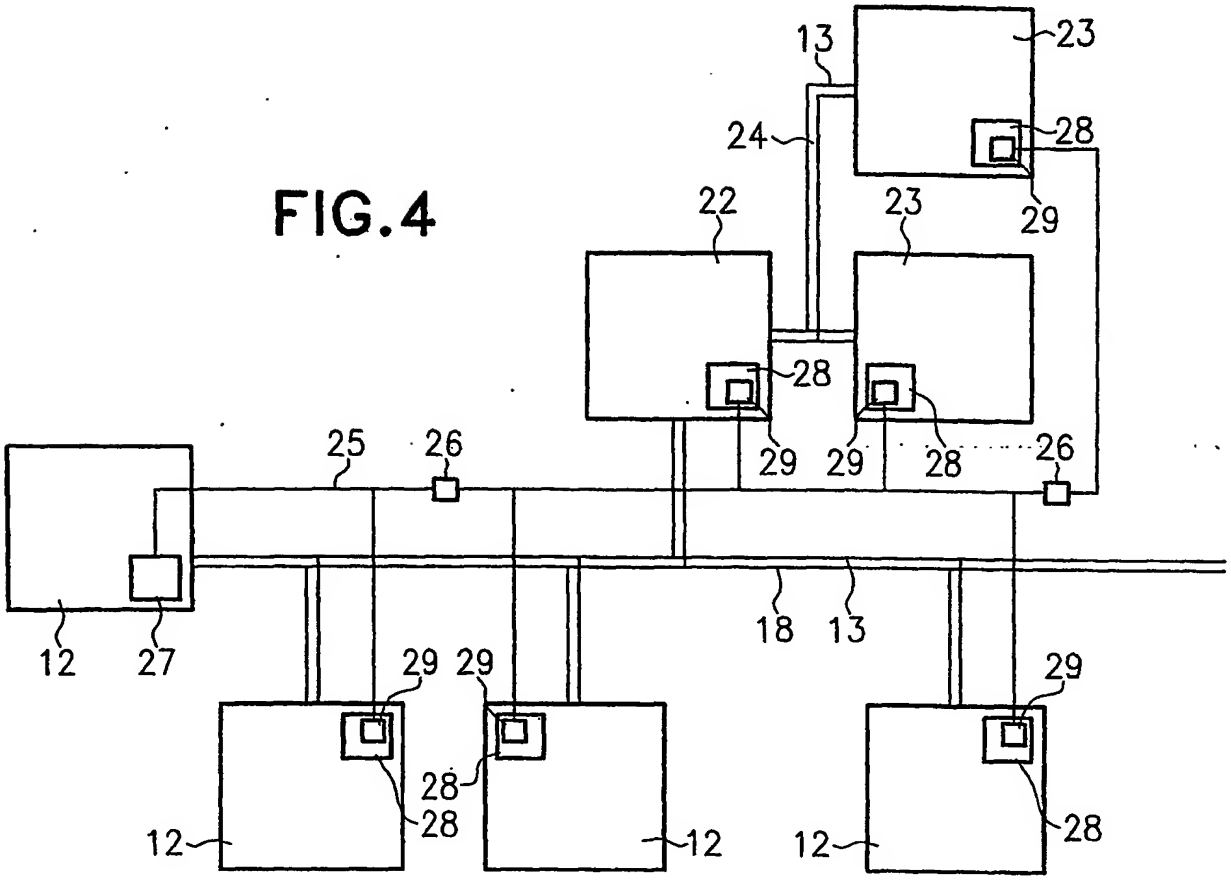


FIG.3

Rec'd PCT/PTO 29 MAR 2005
PCT/EP2003/011087
10/529527

FIG.4



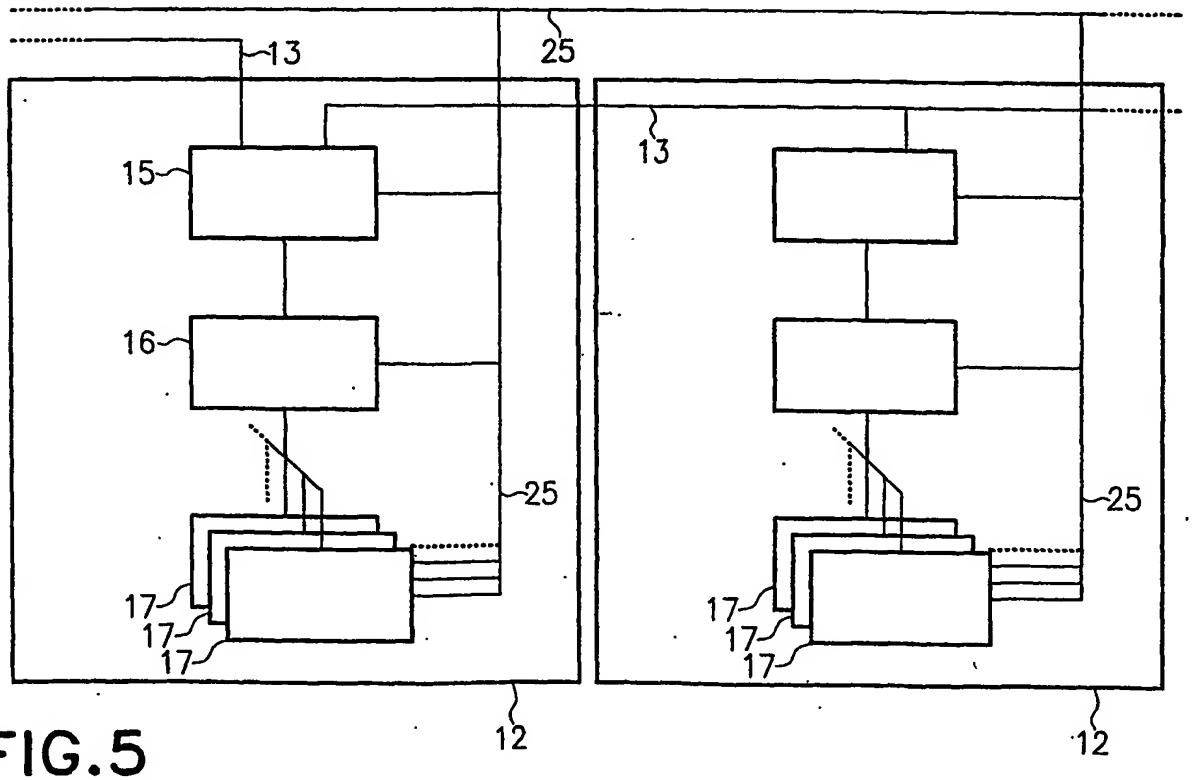


FIG.5

Rec'd PCT/PTO 29 MAR 2005
PCT/EP2003/011087
10/529527

PI_VW	1	PI_SM_PCB3_SAT3	20	PI2_SM_PCB2_SAT2	39
PI_RT	2	PI1_SM_PCB1_BM	21	PI2_SM_PCB2_SAT3	40
PI1_VW	3	PI1_SM_PCB1_SAT1	22	PI2_SM_PCB3_BM	41
PI1_RT	4	PI1_SM_PCB1_SAT2	23	PI2_SM_PCB3_SAT1	42
PI2_VW	5	PI1_SM_PCB1_SAT3	24	PI2_SM_PCB3_SAT2	43
PI2_RT	6	PI1_SM_PCB2_BM	25	PI2_SM_PCB3_SAT3	44
PI3_VW	7	PI1_SM_PCB2_SAT1	26	PI3_SM_PCB1_BM	45
PI3_RT	8	PI1_SM_PCB2_SAT2	27	PI3_SM_PCB1_SAT1	46
PI_SM_PCB1_BM	9	PI1_SM_PCB2_SAT3	28	PI3_SM_PCB1_SAT2	47
PI_SM_PCB1_SAT1	10	PI1_SM_PCB3_BM	29	PI3_SM_PCB1_SAT3	48
PI_SM_PCB1_SAT2	11	PI1_SM_PCB3_SAT1	30	PI3_SM_PCB2_BM	49
PI_SM_PCB1_SAT3	12	PI1_SM_PCB3_SAT2	31	PI3_SM_PCB2_SAT1	50
PI_SM_PCB2_BM	13	PI1_SM_PCB3_SAT3	32	PI3_SM_PCB2_SAT2	51
PI_SM_PCB2_SAT1	14	PI2_SM_PCB1_BM	33	PI3_SM_PCB2_SAT3	52
PI_SM_PCB2_SAT2	15	PI2_SM_PCB1_SAT1	34	PI3_SM_PCB3_BM	53
PI_SM_PCB2_SAT3	16	PI2_SM_PCB1_SAT2	35	PI3_SM_PCB3_SAT1	54
PI_SM_PCB3_BM	17	PI2_SM_PCB1_SAT3	36	PI3_SM_PCB3_SAT2	55
PI_SM_PCB3_SAT1	18	PI2_SM_PCB2_BM	37	PI3_SM_PCB3_SAT3	56
PI_SM_PCB3_SAT2	19	PI2_SM_PCB2_SAT1	38		

FIG.6

Rec'd PCT/PTO 29 MAR 2005
PCT/EP2003/011087

10/529527

Sender \ endg. Empfänger	cs_noexist_proc	PI_VW	PI_RT	PI1_VW	PI1_RT
/*cs_noexist_proc*/	{{{ 0 ,0 }},	{ 0 ,0 },	{ 0 ,0 },	{ 0 ,0 },	{ 0 ,0 },
/* PI_VW */	{{{ 0 ,0 }},	{B_MSG, 0 },	{B_DPR, PI_RT},	{B_CAN, PI1_VW },	{B_CAN, PI1_VW }, ...
/* PI_RT */	{{{ 0 ,0 }},	{B_DPR, PI_VW},	{B_MSG, 0 },	{B_DPR, PI_VW },	{B_DPR, PI_VW}, ...
/* PI1_VW */	{{{ 0 ,0 }},	{B_CAN, PI_VW },	{B_CAN, PI_VW },	{B_MSG, 0 },	{B_DPR, PI1_RT }, ...
/* PI1_RT */	{{{ 0 ,0 }},	{B_DPR, PI1_VW },	{B_DPR, PI1_VW },	{B_DPR, PI1_VW },	{B_MSG, 0 }, ...
/* PI2_VW */	{{{ 0 ,0 }},	{B_CAN, PI_VW },	{B_CAN, PI_VW },	{B_CAN, PI1_VW }	{B_CAN, PI1_VW), ...
/* PI2_RT */	{{{ 0 ,0 }},	{B_DPR, PI2_VW },	{B_DPR, PI2_VW },	{B_DPR, PI2_VW },	{B_DPR, PI2_VW }, ...
/* PI3_VW */	{{{ 0 ,0 }},	{B_CAN, PI_VW },	{B_CAN, PI_VW },	{B_CAN, PI1_VW },	{B_CAN, PI1_VW }, ...
/* PI3_RT */	{{{ 0 ,0 }},	{B_DPR, PI3_VW },	{B_DPR, PI3_VW },	{B_DPR, PI3_VW },	{B_DPR, PI3_VW }, ...
/* PI_SM_PCB1_BM */	{{{ 0 ,0 }},	{B_CAN, PI_RT },	{B_CAN, PI_RT },	{B_CAN, PI_RT },	{B_CAN, PI_RT }, ...
/*PI_SM_PCB1_SAT1*/	{{{ 0 ,0 }},	{B_CAN, PI_RT },	{B_CAN, PI_RT },	{B_CAN, PI_RT },	{B_CAN, PI_RT }, ...

FIG.7